



EXHIBIT 008

U.S. Patent No. 7,373,449 (Radulescu and Goossens)**“Apparatus and method for communicating in an integrated circuit”**

'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
10. Method for exchanging messages in an integrated circuit comprising a plurality of modules,	<p>Without conceding that the preamble of claim 10 of the '449 Patent is limiting, Samsung Galaxy Z Flip 4 (hereinafter, the “Samsung product”) performs a method for exchanging messages in an integrated circuit comprising a plurality of modules, either literally or under the doctrine of equivalents.</p> <p>The Samsung product includes an integrated circuit. For example, the Samsung product includes the Qualcomm Snapdragon 8+ Gen 1 Mobile Platform system on chip (hereinafter, the “Snapdragon SoC”).</p> <div data-bbox="516 639 926 1114">  </div> <div data-bbox="1131 630 1806 695"> <h2>Samsung Galaxy Z Flip4</h2> </div> <div data-bbox="1131 711 1736 743"> <p>Powered by Snapdragon 8+ Gen 1 Mobile Platform</p> </div> <div data-bbox="1131 768 1860 1105"> <p>Get the phone that claps back. The Snapdragon 8+ Gen 1 powered Galaxy Z Flip4 from Samsung Mobile has launched in style. This sleek, pocket-sized smartphone allows you to snap hands-free photos with Flex Cam, makes checking notifications a breeze with its cover screen, and comes in a wide array of colors. Plus, take selfies with the Rear Camera while the Cover Screen gives you a real-time preview. Check yourself from afar with a full-screen view finder, or tap to see the original ratio to make sure everyone is in frame.</p> </div> <div data-bbox="499 1130 1673 1169"> <p>https://www.qualcomm.com/snapdragon/device-finder/samsung-galaxy-z-flip4</p> </div>

¹ The Samsung product is charted as a representative product made used, sold, offered for sale, and/or imported by Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.


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'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>The Snapdragon SoC comprises a plurality of modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):</p> <div data-bbox="514 410 947 553">  <p>Snapdragon 8+ mobile platform Gen 1</p> </div> <div data-bbox="1562 440 1869 459">SPECIFICATIONS & FEATURES</div> <div data-bbox="514 630 741 652"> <p>Artificial Intelligence</p> <hr/> <p>Qualcomm® Adreno™ GPU</p> <hr/> <p>Qualcomm® Kryo™ CPU</p> <hr/> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> • Fused AI Accelerator • Hexagon Tensor Accelerator • Hexagon Vector eXtensions • Hexagon Scalar Accelerator • Support for mix precision(INT8+INT16) • Support for all precisions (INT8, INT16, FP16) <hr/> <p>Qualcomm® Sensing Hub</p> <hr/> <p>5G Modem-RF System</p> <hr/> <p>Snapdragon® X65 5G Modem-RF System</p> <ul style="list-style-type: none"> • 5G mmWave and sub-6 GHz, standalone • (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 8 carriers, 2x2 MIMO • Sub-6 GHz: 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM <hr/> <p>Downlink: Up to 10 Gbps</p> <hr/> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE</p> <hr/> <p>Camera</p> <hr/> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture <hr/> <p>Rec. 2020 color gamut photo and video capture</p> <hr/> <p>Up to 10-bit color depth photo and video capture</p> <hr/> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <hr/> <p>10-bit HEIF™: HEIC photo capture, HEVC video capture</p> <hr/> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <hr/> <p>8K HDR Video Capture @ 30 FPS</p> <hr/> <p>4K Video Capture @ 120 FPS</p> <hr/> <p>Slow-mo video capture at 720p @ 960 FPS</p> <hr/> <p>Bokeh Engine for Video Capture</p> <hr/> <p>Video super resolution</p> <hr/> <p>Multi-frame Noise Reduction (MFNR)</p> <hr/> <p>Locally Motion Compensated Temporal Filtering</p> <hr/> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <hr/> <p>AI-based face detection, auto-focus, and</p> <hr/> <p>CPU</p> <hr/> <p>Kryo CPU</p> <ul style="list-style-type: none"> • Up to 3.2 GHz*, with Arm Cortex-X2 technology • 64-bit Architecture <hr/> <p>Visual Subsystem</p> <hr/> <p>Adreno GPU</p> <ul style="list-style-type: none"> • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision <hr/> <p>Security</p> <hr/> <p>Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU)</p> <hr/> <p>Trust Management Engine</p> <hr/> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <hr/> <p>Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor)</p> <hr/> <p>Qualcomm® Type-1 Hypervisor</p> <hr/> </div>

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	<div data-bbox="506 250 934 901"> <p>Wi-Fi & Bluetooth*</p> <hr/> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), • Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal <hr/> <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> • Bluetooth Features: Bluetooth® 5.3, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio <hr/> <p>snapdragon.com</p> </div> <div data-bbox="976 250 1404 771"> <p>Audio</p> <hr/> <p>Qualcomm Aqstic™ audio codec (WCD9385)</p> <p>New Qualcomm Aqstic smart speaker amplifier (WSA8835)</p> <p>Total Harmonic Distortion + Noise (THD+N), Playback: -108dB</p> <p>Qualcomm® Audio and Voice Communication Suite</p> <hr/> <p>Display</p> <hr/> <p>On-Device Display Support:</p> <ul style="list-style-type: none"> • 4K @ 60 Hz • QHD+ @ 144 Hz <hr/> <p>Maximum External Display Support: up to 4K @ 60 Hz</p> <ul style="list-style-type: none"> • 10-bit color depth, Rec. 2020 color gamut • HDR10 and HDR10+ <hr/> <p>Demura and subpixel rendering for OLED Uniformity</p> </div> <div data-bbox="1446 250 1875 868"> <p>Charging</p> <hr/> <p>Qualcomm® Quick Charge™ 5 Technology</p> <hr/> <p>Location</p> <hr/> <p>GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable</p> <hr/> <p>Dual Frequency GNSS (L1/L5)</p> <hr/> <p>Sensor-Assisted Positioning</p> <ul style="list-style-type: none"> • Urban pedestrian navigation with sidewalk accuracy • Global freeway lane-level vehicle navigation <hr/> <p>Memory</p> <hr/> <p>Support for LP-DDR5 memory up to 3200 MHz</p> <hr/> <p>Memory Density: up to 16 GB</p> <hr/> <p>General Specifications</p> <hr/> <p>Full Suite of Snapdragon Elite Gaming™ features</p> <hr/> <p>4 nm Process Technology</p> <hr/> <p>USB Version 3.1; USB Type-C Support</p> <hr/> <p>Part Number: SM8475</p> </div> <div data-bbox="506 933 1885 1092" style="background-color: #2c3e50; color: white; padding: 10px; font-size: 0.8em;"> <p>*Snapdragon 8+ Gen 1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed.</p> <p>Certain optional features available subject to Carrier and OEM selection for an additional fee.</p> <p>Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Kiyo, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Aqstic, Qualcomm 3D Sonic Sensor, Qualcomm Type-1 Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries.</p> <p>Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kiyo, Smart Transmit, Qualcomm Spectra, Qualcomm Aqstic, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd.</p> <p>©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</p> </div> <div data-bbox="493 1130 1463 1209" data-label="Text"> <p>https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf</p> </div> <div data-bbox="493 1248 1751 1367" data-label="Text"> <p>The Snapdragon SoC included in the Samsung product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) to exchange messages:</p> </div>

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	<div><p>Qualcomm</p><p></p><p>Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</p><p>LEARN MORE »</p></div> <p>https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</p>

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'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹ Certain Arteris Technology Assets Acquired
	<p>by Kurt Shuler, on October 31, 2013</p> <p>Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p>SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p>“Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology.</p> <p>ARTERIS</p> <p><i>K. Charles Janac, President and CEO, Arteris</i></p> <p>https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</p> <p>The Arteris NoC exchanges messages in the Snapdragon SoC included in the Samsung product.</p> <p>For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

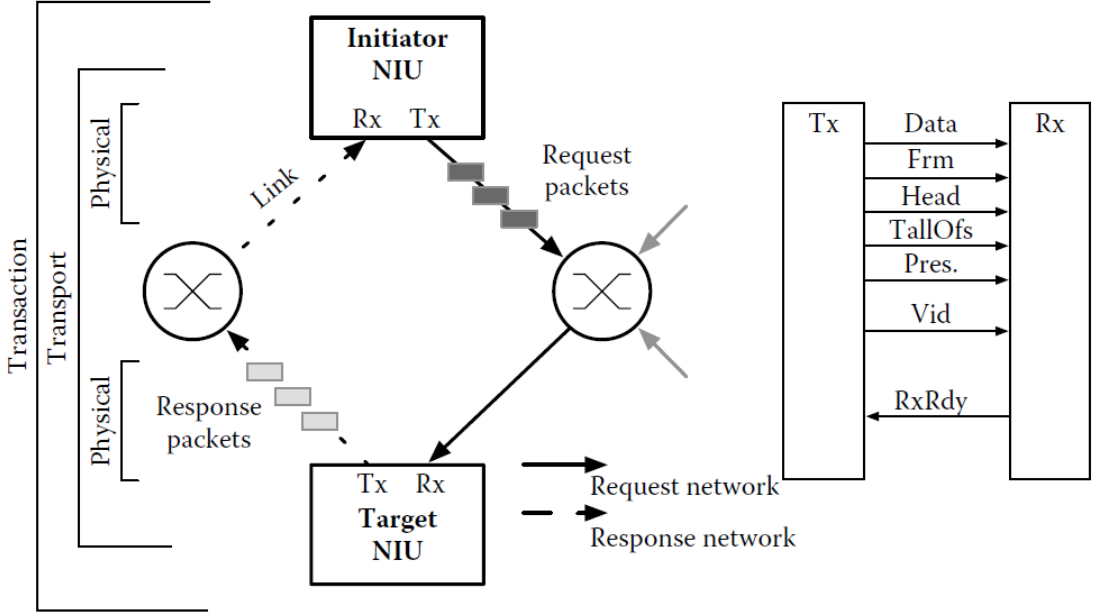
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	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p>
the messages between the modules being	Without conceding that the preamble of claim 10 of the '449 Patent is limiting, the Arteris NoC exchanges messages between modules in the Snapdragon SoC included in the Samsung product over connections via a network, wherein said connections comprises a set of communication

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exchanged over connections via a network, wherein said connections comprises a set of communication channels each having a set of connection properties, any communication channel being independently configurable,

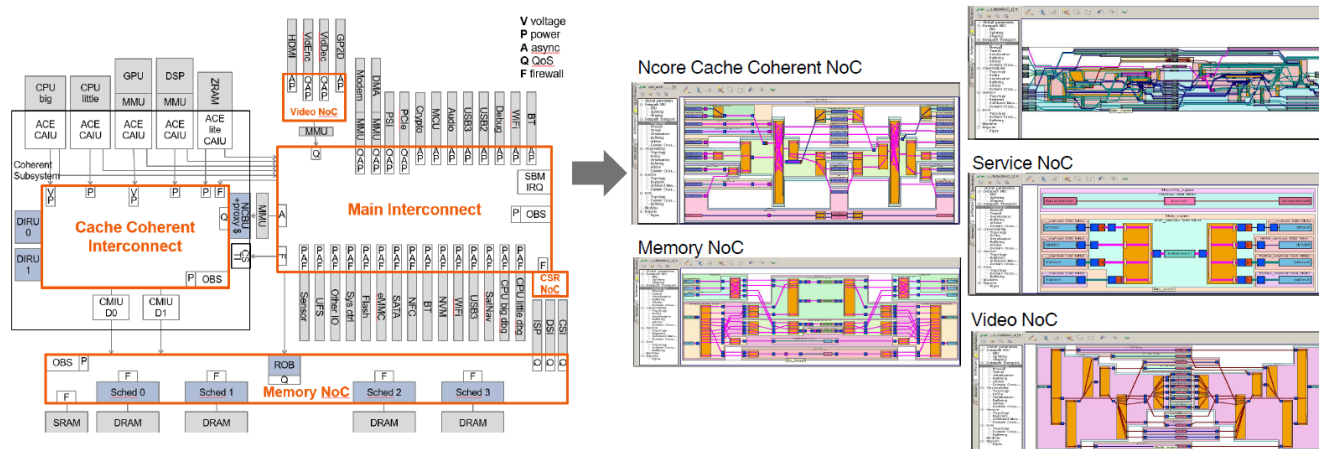
Samsung Product Including Snapdragon System on Chip¹

channels each having a set of connection properties any communication channel being independently configurable, either literally or under the doctrine of equivalents.

A large SoC, such as the Snapdragon SoC included in the Samsung product may include multiple classes of Arteris NoC interconnect network:

Logical Interconnect Topology Development

FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES



- ArChip16 Example: Large SoCs have multiple classes of interconnect
 - Non-coherent, Coherent, Control/Status, Observability, etc.
- Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility

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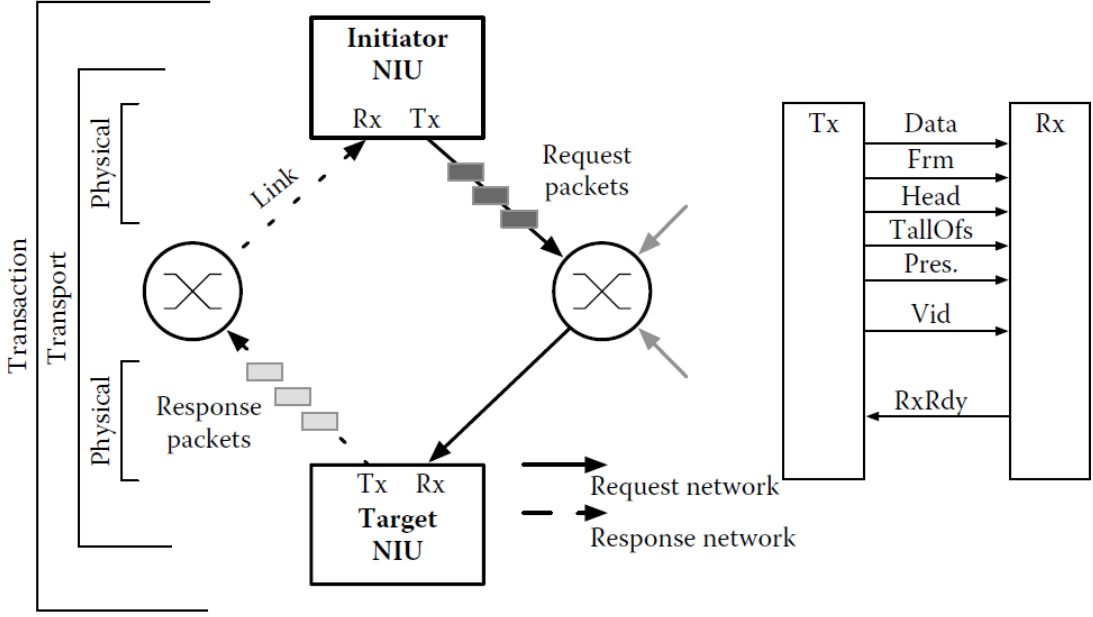
See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

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	<p>The Snapdragon SoC included in the Samsung product utilizes the Arteris NoC to exchange messages over connections via a network, wherein said connections comprises a set of communication channels that are independently configurable.</p> <p>For example, in the the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>Connections within the Arteris NoC network may be defined by a connectivity table:</p>

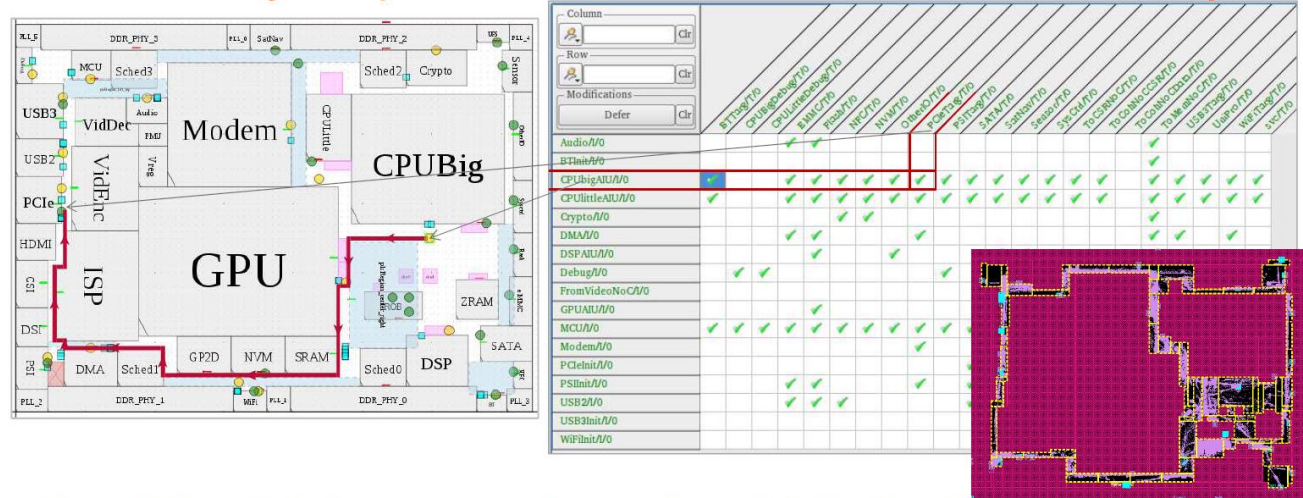
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Connectivity Map → Interconnect Connections → Layout



DC-Topographical

- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.

In the Arteris NoC, “[t]he delivery of packets within the NoC is the responsibility of the physical layer [where the] link size, or width (i.e., number of wires), is set by the designer at design time[and] [o]ne link (represented in Figure 11.1) defines the following signals... Pres. – Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2) [and] RxRdy – flow control”:

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	<p>11.3.1.3 Physical Layer</p> <p>The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on. Words travel within point-to-point links, which are independent from other protocol layers: a word is sent through a transmit port, Tx, over a link to a receive port, Rx. The actual number of wires in a link depends on the</p>

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maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in [Figure 11.1](#)) defines the following signals:

- **Data**—Data word of the width specified at design-time.
- **Frm**—When asserted high, indicates that a packet is being transmitted.
- **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.
- **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.
- **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in [Figure 11.2](#)).
- **Vld**—Data valid: when asserted high, indicates that a word is being transmitted.
- **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy.

This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTPP communications.

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	<p data-bbox="499 289 1856 365"><i>See</i> Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313-314.</p> <p data-bbox="499 409 1881 524">The Snapdragon SoC included in the Samsung product utilizes the Arteris NoC's connections that comprise a set of communication channels each having a set of connection properties, any communication channel being independently configurable.</p> <p data-bbox="499 568 1877 683">For example, as noted above, in the Arteris NoC, “[o]ne link (represented in Figure 11.1) defines the following signals... Pres. – Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service) [and] RxRdy – flow control.”</p> <p data-bbox="499 727 1818 803">In the Arteris NoC implements Quality of Service (QoS) to “provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic”:</p> <p data-bbox="520 857 1835 1226">Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in <i>Æthereal</i> NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p data-bbox="520 1234 1835 1323">In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> • Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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	<p data-bbox="541 282 1843 354">* Note that in the NTTP packet, the pressure field allows more than one bit, resulting in multiple levels of preferred traffic.</p> <p data-bbox="499 386 1801 457">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.</p> <p data-bbox="499 506 1759 578">As a further illustration, the Arteris NoC “addresses ... varied QoS needs in many ways,” including “Dynamic Packet Priorities” and “Dynamic Pressure Propagation”:</p> <h2 data-bbox="541 630 1671 766">Arbitration: Dynamic Packet Priorities & Dynamic Pressure Propagation</h2> <p data-bbox="541 831 1696 1052">Arteris Network on Chip technology addresses these varied QoS needs in many ways: First, the interconnect assigns priorities to transactions to ensure they arrive at the target in the proper order to meet system requirements. Priority levels can be attached to individual packets or to all transactions pending on a socket. The interconnect can also assign Dynamic Packet Priorities at runtime.</p> <p data-bbox="541 1117 1667 1338">Second, the interconnect can sense when high priority packets may be blocked or slowed due to downstream traffic congestion and can then clear a path for these high priority packets. This technology, called Dynamic Pressure Propagation, is analogous to a fire truck racing down city streets: All traffic pulls to the side of the road to let the fire truck through.</p> <p data-bbox="499 1370 1356 1403">https://www.arteris.com/end-to-end-quality-of-service-qos</p>

U.S. Patent No. 7,373,449 (Radulescu and Goossens)**“Apparatus and method for communicating in an integrated circuit”**

'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>As a further illustration, “QoS information may be generated from within the [Arteris] NoC interconnect using Arteris’ QoS Generator”:</p> <h2 data-bbox="527 418 1478 483">Bandwidth Limiters and Rate Regulators</h2> <p>Many times architects will want to implement QoS within their SoC but the QoS prioritization data is not available from the individual IP blocks. In this case, QoS information may be generated from within the NoC interconnect using Arteris’ QoS Generator. The QoS Generator can instantiate sophisticated, and software programmable, means to regulate interconnect QoS, including:</p> <ul style="list-style-type: none"> ➤ Bandwidth Limiters – Bandwidth limiters cause a socket to stop accepting requests when a run-time programmable throughput threshold has been exceeded. ➤ Rate Regulators – Rate regulators cause a socket’s transactions to be demoted when a bandwidth threshold is reached. This can be considered a smoother version of the bandwidth limiter because transactions are only demoted instead of stalled. <p>https://www.arteris.com/end-to-end-quality-of-service-qos</p> <p>As a further illustration, the Arteris NoC uses “a mechanism called rated adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.” For other traffic, the “[b]est effort traffic can be left untouched[,]” “[l]atency sensitive traffic may have its</p>

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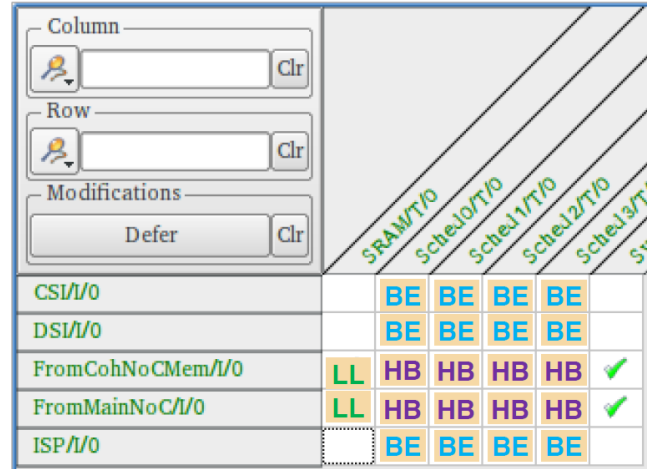
'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>urgency modulated as a function of the transaction[,]” “[s]oft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives[,]” and “[o]n the real-time modem data port, the hurry is fixed at a critical level”:</p> <p>Those effects can be mended by the insertion of buffering. In the case of peak bandwidth reduction, a simple FIFO does the job: Busy states present at the output of the FIFO do not propagate back to the input until the FIFO is full. For a peak bandwidth increase, the situation is a bit more complex. In a FIFO, wait states present at the input are only absorbed when the FIFO is not empty. Arteris proposes a mechanism called rate adaptation, which stalls packets just enough to remove wait states from the packets, preserving a low latency.</p> <p>In this second step, the architecture is modified to introduce some buffering. In our example 760 bytes of memory have been distributed across the topology. Some have been put on existing links; some required the creation of new links.</p> <p>See Application driven network-on-chip architecture exploration & refinement for a complex SoC, https://www.arteris.com/hs-fs/hub/48858/file-14363521-pdf/docs/springerappdrivennocarchitecture8.5x11.pdf, at pg.16.</p> <p>For the other traffic, “the configuration can be done in architecture”:</p>

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	<ul style="list-style-type: none"> • Best effort traffic can be left untouched. • Latency sensitive traffic may have its urgency modulated as a function of the transaction: <i>Normal</i> for writes and <i>important</i> for reads. • Soft real-time traffic may have its hurry level modulated as a function of the bandwidth it receives: <i>Critical</i> until a specified bandwidth is obtained on a sliding 4 microsecond window, and <i>normal</i> thereafter. These settings are set through configuration registers and may be modified while the interconnect is running. The mechanism is called a bandwidth regulator. • On the real-time modem data port, the hurry is fixed at a critical level. <p><i>Id.</i> at 18.</p> <p>As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes may be mapped onto the Arteris interconnect topology:</p>

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'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹						
	<p data-bbox="533 284 1463 381">Memory NoC: Interconnect Topology – Traffic Classes</p> <p data-bbox="533 440 1066 500">Classify your IP connections per class of traffic:</p> <table data-bbox="533 553 1119 686"> <tr> <td>Best Effort (BE)</td><td>Image system</td></tr> <tr> <td>Low Latency (LL)</td><td>SRAM</td></tr> <tr> <td>High Bandwidth (HB)</td><td>Main/Coherency</td></tr> </table> <div data-bbox="1163 469 1806 935">  <p>The screenshot shows a configuration window with a control panel on the left and a traffic class matrix on the right. The control panel includes fields for 'Column' and 'Row' with search icons and 'Clr' buttons, and a 'Modifications' section with a 'Defer' button and a 'Clr' button. The matrix has rows for IP blocks: CSI/I/O, DSI/I/O, FromCohNoCMem/I/O, FromMainNoC/I/O, and ISP/I/O. The columns represent traffic classes: BE (Best Effort), LL (Low Latency), and HB (High Bandwidth). The matrix shows that CSI/I/O and DSI/I/O are assigned BE. FromCohNoCMem/I/O and FromMainNoC/I/O are assigned LL and HB. ISP/I/O is assigned BE. Checkmarks are visible in the bottom right of the matrix for the FromCohNoCMem/I/O and FromMainNoC/I/O rows.</p> </div>	Best Effort (BE)	Image system	Low Latency (LL)	SRAM	High Bandwidth (HB)	Main/Coherency
Best Effort (BE)	Image system						
Low Latency (LL)	SRAM						
High Bandwidth (HB)	Main/Coherency						
<div data-bbox="499 998 1885 1068"> <div data-bbox="499 1015 636 1044">ARTERIS^{IP}</div> <div data-bbox="1092 1019 1247 1037">ISPD 2018, 28 March 2018</div> <div data-bbox="1629 1019 1862 1037">Copyright © 2018 Arteris IP 13</div> </div>							

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	<p>Memory NoC: Traffic classes are mapped onto logical interconnect topology</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="border: 1px solid black; padding: 5px; width: 45%;"> <p>Column <input type="text"/> <input type="button" value="Clr"/></p> <p>Row <input type="text"/> <input type="button" value="Clr"/></p> <p>Modifications <input type="button" value="Defer"/> <input type="button" value="Clr"/></p> <table border="1"> <thead> <tr> <th></th> <th>SRAM/T/O</th> <th>Sched0/T/O</th> <th>Sched1/T/O</th> <th>Sched2/T/O</th> <th>Sched3/T/O</th> <th>Sched4/T/O</th> </tr> </thead> <tbody> <tr> <td>CSI/I/O</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> <td></td> </tr> <tr> <td>DSI/I/O</td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> <td></td> </tr> <tr> <td>FromCohNoCMem/I/O</td> <td>LL</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>✓</td> </tr> <tr> <td>FromMainNoC/I/O</td> <td>LL</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>HB</td> <td>✓</td> </tr> <tr> <td>ISP/I/O</td> <td></td> <td>BE</td> <td>BE</td> <td>BE</td> <td>BE</td> <td></td> </tr> </tbody> </table> </div> <div style="width: 50%;"> </div> </div>		SRAM/T/O	Sched0/T/O	Sched1/T/O	Sched2/T/O	Sched3/T/O	Sched4/T/O	CSI/I/O	BE	BE	BE	BE			DSI/I/O	BE	BE	BE	BE			FromCohNoCMem/I/O	LL	HB	HB	HB	HB	✓	FromMainNoC/I/O	LL	HB	HB	HB	HB	✓	ISP/I/O		BE	BE	BE	BE	
	SRAM/T/O	Sched0/T/O	Sched1/T/O	Sched2/T/O	Sched3/T/O	Sched4/T/O																																					
CSI/I/O	BE	BE	BE	BE																																							
DSI/I/O	BE	BE	BE	BE																																							
FromCohNoCMem/I/O	LL	HB	HB	HB	HB	✓																																					
FromMainNoC/I/O	LL	HB	HB	HB	HB	✓																																					
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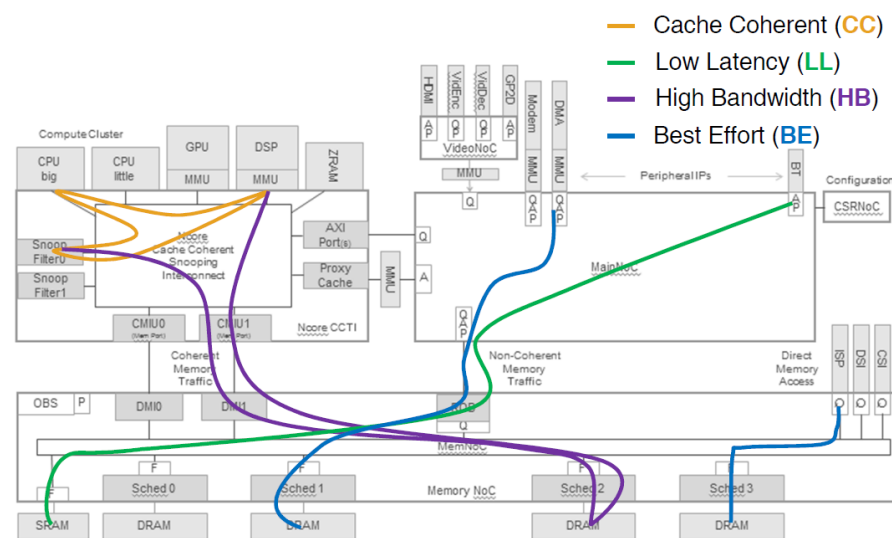
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'449 Patent Claim**Samsung Product Including Snapdragon System on Chip¹****Memory Access Traffic Classes**

- **Cache Coherent (CC)** within Compute Cluster
- **Low Latency (LL)** to SRAM
- **High Bandwidth (HB)** to DRAM & Cache Fill
- **Best Effort (BE)** for Peripherals & DMA
- QoS for Video
- Multiple functional NoCs interacting
- Physically Constrained

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.

As a further illustration, in the Arteris NoC, “QoS is supported in the switch using pressure information generated by the IP itself and embedded in NTTP packets” and “[s]ome features [of the switch] can be software-controlled at runtime through the service network”:

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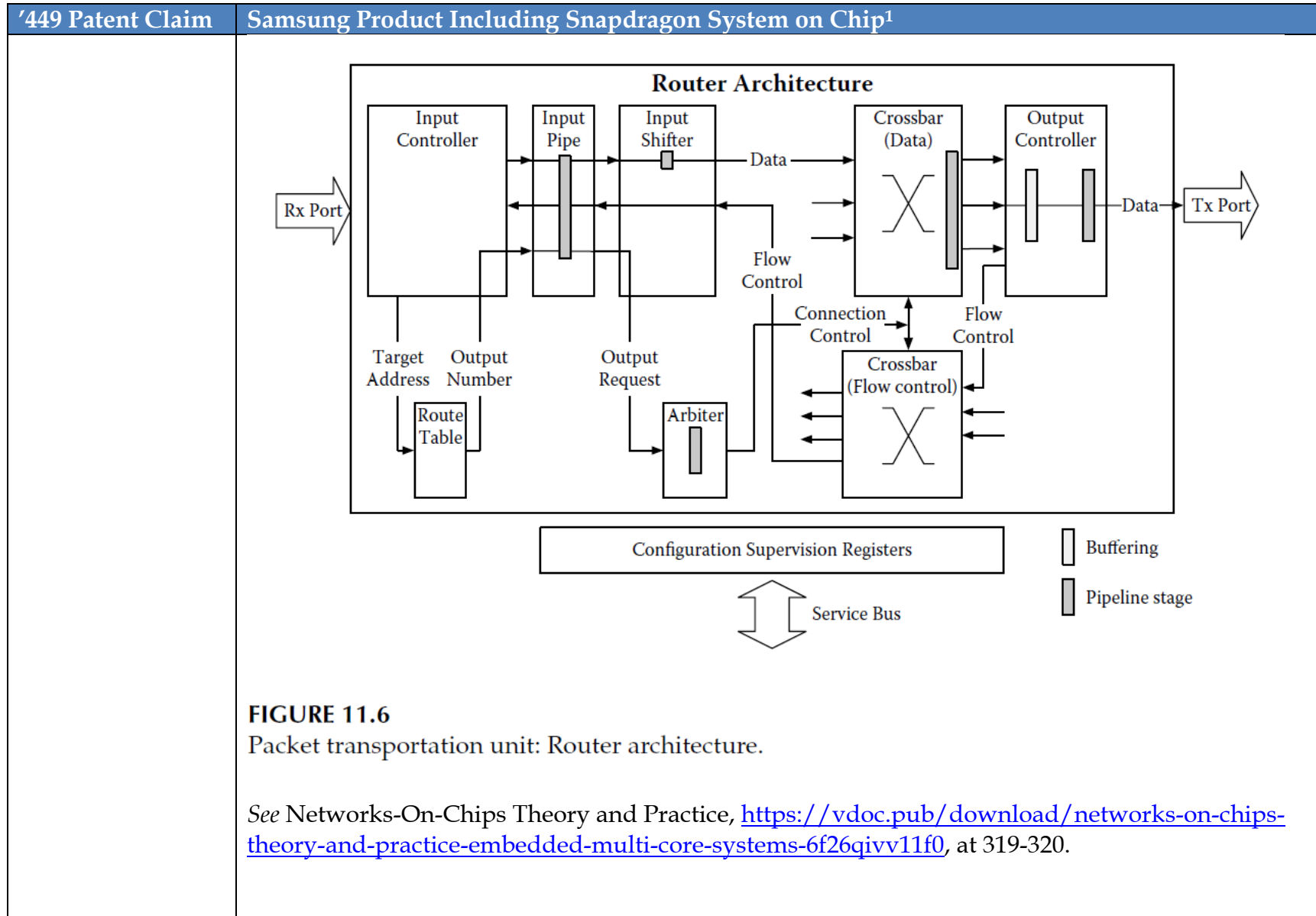
'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>11.3.3.1 Switching</p> <p>The switching is done by accepting NTTP packets carried by input ports and forwarding each packet transparently to a specific output port. The switch is characterized with a fully synchronous operation and can be implemented as a full crossbar (up to one data word transfer per port and per cycle), although there is an automatic removal of hardware corresponding to unused input/output port connections (port depletion). The switch uses wormhole routing, for reduced latency, and can provide full throughput arbitration; that is, up to one routing decision per input port and per cycle. An arbitrary number of switches can be connected in cascade, supporting any loopless network topology. The QoS is supported in the switch using the pressure information generated by the IP itself and embedded in NTTP packets.</p> <p>A switch can be configured to meet specific application requirements by setting the MINI-ports (Rx or Tx ports, as defined by the MINI interface introduced earlier) attributes, routing tables, arbitration mode, and pipelining strategy. Some of the features can be software-controlled at runtime through</p>

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	<p>the service network. There is one routing table per Rx port and one arbiter per Tx port. Packet switching consists of the following four stages:</p> <ol style="list-style-type: none"> 1. Choosing the route—Using relevant information extracted from the packet, the routing table selects a target output port. 2. Arbitrating—Because more than a single input port can request a given output port at a given time, an arbiter selects one requesting input port per output port. The arbiter maintains input/output connection until the packet completes its transit in the switch. 3. Switching—Once routing and arbitration decisions have been made, the switch transports each word of the packet from its input port to its output port. The switch implementation employs a full crossbar, ensuring that the switch does not contribute to congestion. 4. Arbiter release—Once the last word of a packet has been pipelined into the crossbar, the arbiter releases the output, making it available for other packets that may be waiting at other input ports. <p>The simplified block diagram of the switch architecture is shown in Figure 11.6.</p>

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	<p>As a further illustration, the “Pres.” signal in the NTTP packet “[i]ndicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2).”</p> <p>FIGURE 11.2 NTTP packet structure.</p> <p><i>See id.</i> at 313, 314.</p> <p>As a further illustration, in the Arteris NoC, “the routing tables actually used in the switch are parameterizable for each input port of the switch. It is thus possible to use different routing tables for each switch input. Routing tables can optionally be programmed via the service network interface; in this case, their configuration registers appear in the switch register address map.”</p> <p><i>See id.</i> at 322.</p>

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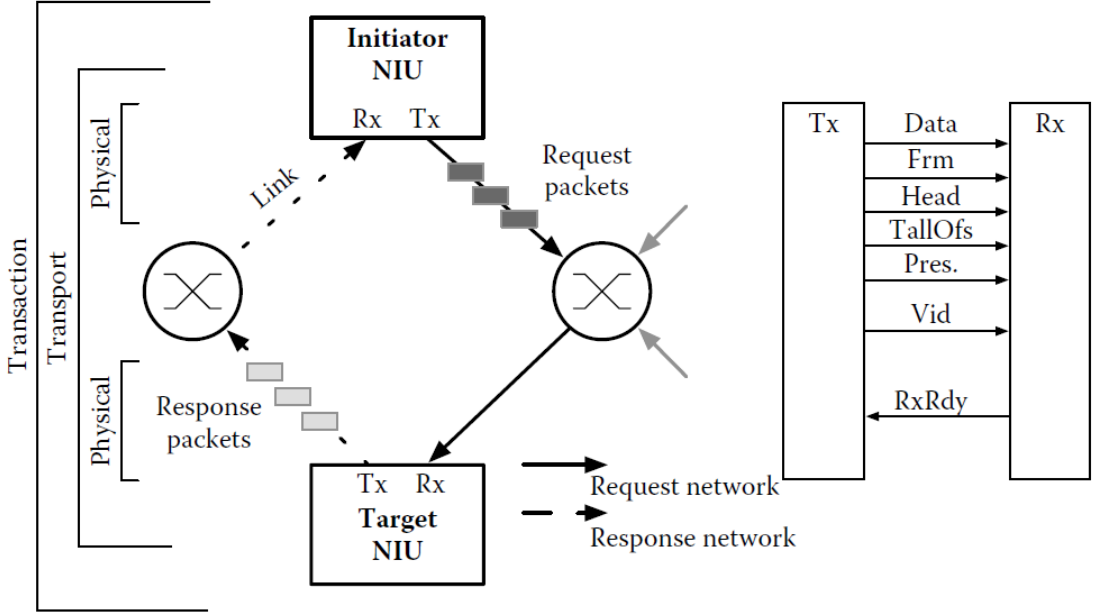
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<p>wherein said connection through the network supports transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module</p>	<p>Without conceding that the preamble of claim 10 of the '449 Patent is limiting, the Arteris NoC in the Snapdragon SoC included in the Samsung product has connections through the network that support transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Snapdragon SoC included in the Samsung product, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p>
and further comprising the steps of: the first module issuing a request	In the Arteris NoC in the Snapdragon SoC included in the Samsung product, the first module issues a request for a connection with the second module to a communication manager, wherein the request comprises desired connection properties associated with the sets of communication channels, either literally or under the doctrine of equivalents.

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for a connection with the second module to a communication manager, wherein the request comprises desired connection properties associated with the sets of communication channels;	<p>The first module of the Snapdragon SoC included in the Samsung product utilizes the Arteris NoC to issue a request for a connection with the second module to a communication manager.</p> <p>For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

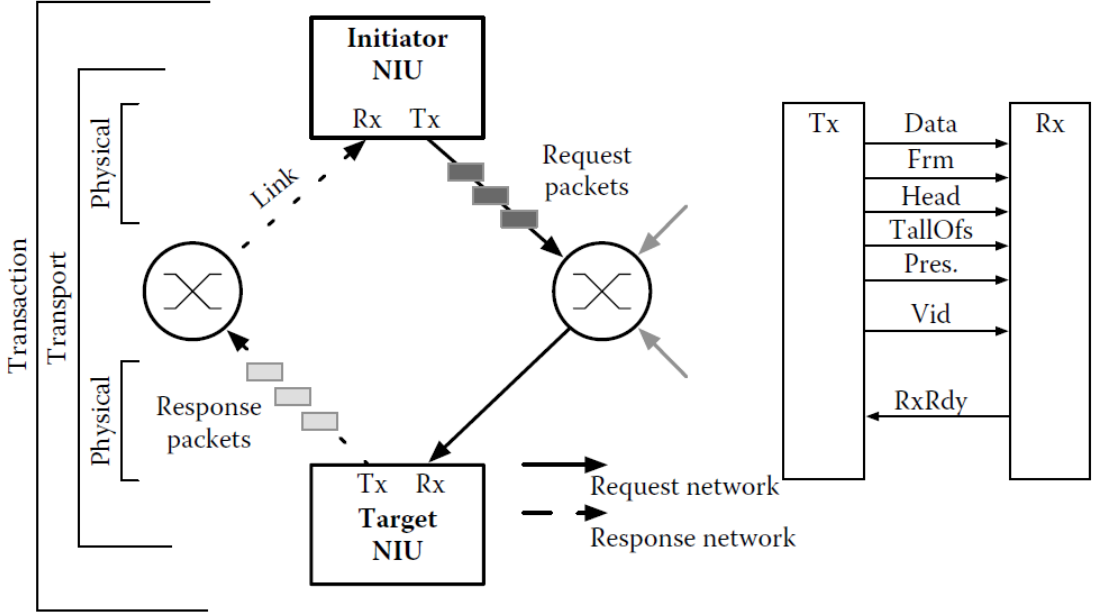
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'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>The request issued by first module of the Snapdragon SoC included in the Samsung product comprises desired connection properties associated with the sets of communication channels.</p> <p>For example, in the Arteris NoC, “[t]he delivery of packets within the NoC is the responsibility of the physical layer [where the] link size, or width (i.e., number of wires), is set by the designer at design time[and] [o]ne link (represented in Figure 11.1) defines the following signals... Pres.—</p>

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	<p>Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2) [and] RxRdy – flow control”:</p> <p>11.3.1.3 Physical Layer</p> <p>The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on. Words travel within point-to-point links, which are independent from other protocol layers: a word is sent through a transmit port, Tx, over a link to a receive port, Rx. The actual number of wires in a link depends on the</p>

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maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in [Figure 11.1](#)) defines the following signals:

- **Data**—Data word of the width specified at design-time.
- **Frm**—When asserted high, indicates that a packet is being transmitted.
- **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.
- **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.
- **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in [Figure 11.2](#)).
- **Vld**—Data valid: when asserted high, indicates that a word is being transmitted.
- **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy.

This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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	<p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313-314.</p> <p>As a further example, in the Arteris NoC, “QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition” where the “pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed” and the “pressure information will be embedded in the NTTP packet at the NIU level”:</p> <p>Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in <i>Æthereal NoC</i> [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p>In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> • Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>* Note that in the NTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.</p> <p>FIGURE 11.2 NTP packet structure.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 315-316.</p> <p>As a further example, in the Arteris NoC, “QoS is supported in the switch using pressure information generated by the IP itself and embedded in NTP packets” and the router architecture includes blocks such as “Input Controller,” “Flow Control,” “Crossbar (Flow control)” “Route Table” and “Arbiter”:</p>

U.S. Patent No. 7,373,449 (Radulescu and Goossens)*“Apparatus and method for communicating in an integrated circuit”*

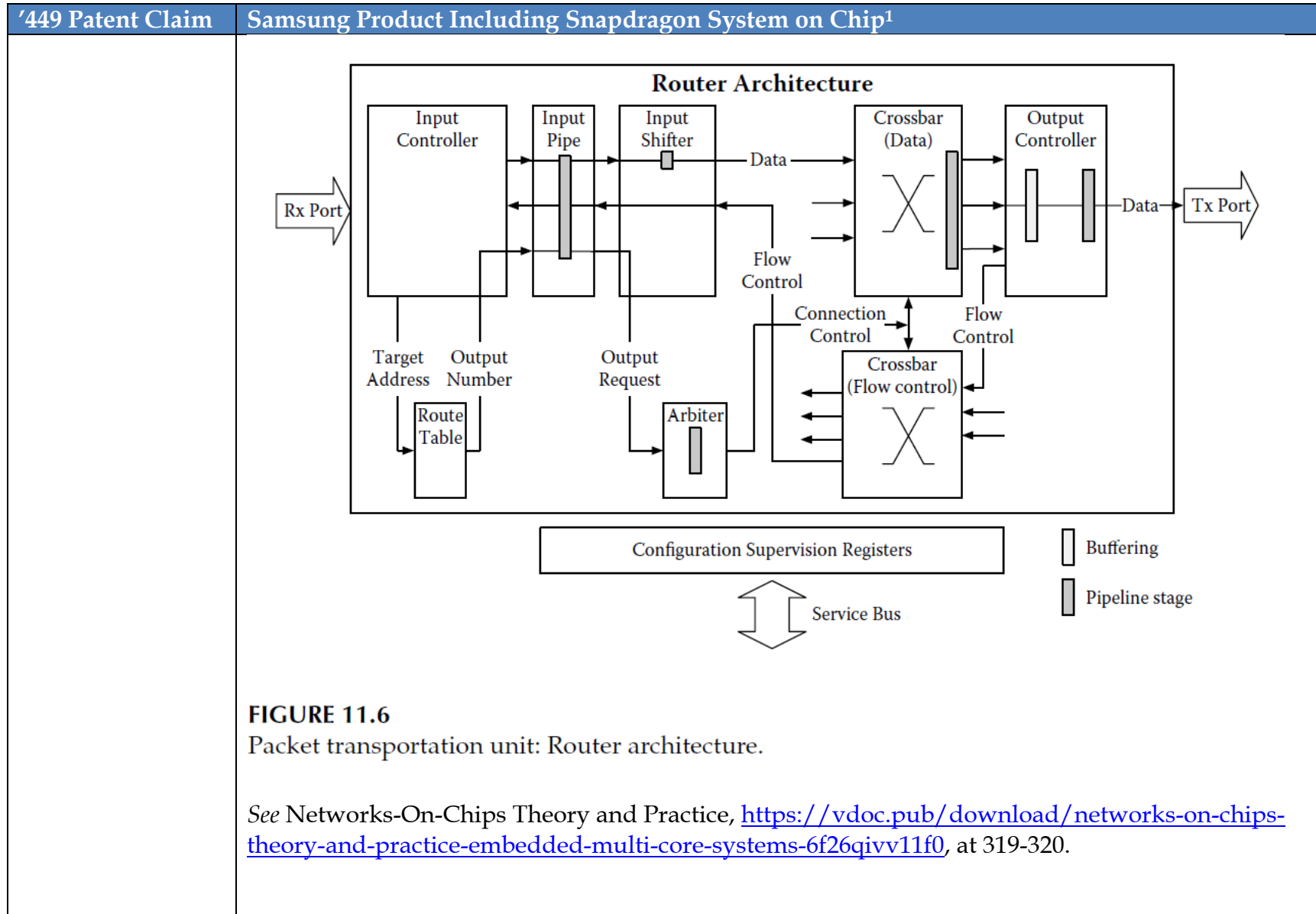
'449 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>11.3.3.1 Switching</p> <p>The switching is done by accepting NTTP packets carried by input ports and forwarding each packet transparently to a specific output port. The switch is characterized with a fully synchronous operation and can be implemented as a full crossbar (up to one data word transfer per port and per cycle), although there is an automatic removal of hardware corresponding to unused input/output port connections (port depletion). The switch uses wormhole routing, for reduced latency, and can provide full throughput arbitration; that is, up to one routing decision per input port and per cycle. An arbitrary number of switches can be connected in cascade, supporting any loopless network topology. The QoS is supported in the switch using the pressure information generated by the IP itself and embedded in NTTP packets.</p> <p>A switch can be configured to meet specific application requirements by setting the MINI-ports (Rx or Tx ports, as defined by the MINI interface introduced earlier) attributes, routing tables, arbitration mode, and pipelining strategy. Some of the features can be software-controlled at runtime through</p>

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	<p>the service network. There is one routing table per Rx port and one arbiter per Tx port. Packet switching consists of the following four stages:</p> <ol style="list-style-type: none"> 1. Choosing the route—Using relevant information extracted from the packet, the routing table selects a target output port. 2. Arbitrating—Because more than a single input port can request a given output port at a given time, an arbiter selects one requesting input port per output port. The arbiter maintains input/output connection until the packet completes its transit in the switch. 3. Switching—Once routing and arbitration decisions have been made, the switch transports each word of the packet from its input port to its output port. The switch implementation employs a full crossbar, ensuring that the switch does not contribute to congestion. 4. Arbiter release—Once the last word of a packet has been pipelined into the crossbar, the arbiter releases the output, making it available for other packets that may be waiting at other input ports. <p>The simplified block diagram of the switch architecture is shown in Figure 11.6.</p>

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the communication manager forwarding the request to a resource manager; the resource manager determining whether a target connection with the desired connection properties is available;	<p>In the Arteris NoC in the Snapdragon SoC included in the Samsung product, the communication manager forwards the request to a resource manager and the resource manager determines whether a target connection with the desired connection properties is available, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by Snapdragon SoC included in the Samsung product, “QoS is supported in the switch” which “choos[es] the route” using a “routing table”; “arbitrat[es]”; and “switch[es]” and the router architecture includes blocks such as “Input Controller,” “Flow Control,” “Crossbar (Flow control)” “Route Table” and “Arbiter”:</p>

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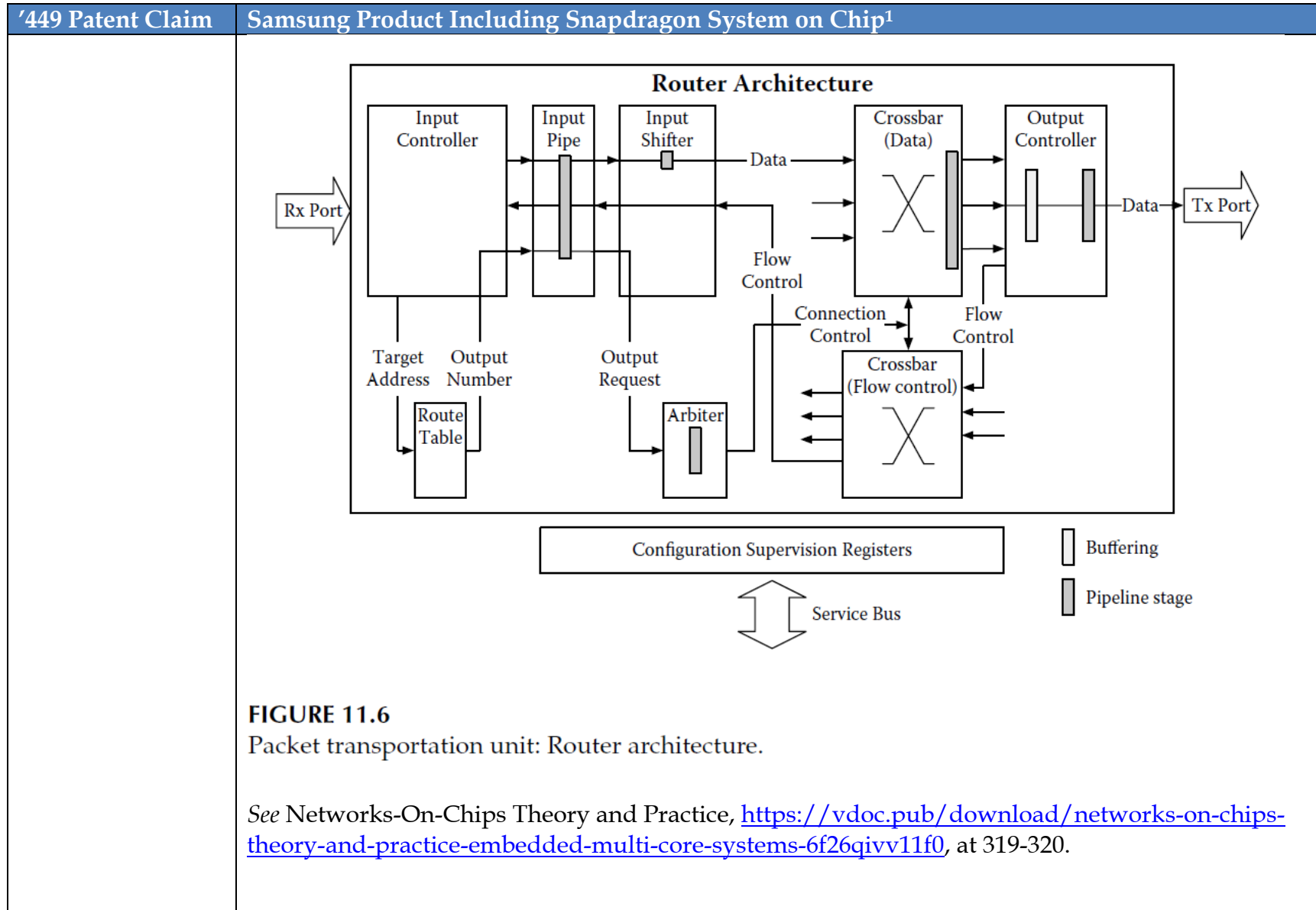
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	<p>As a further illustration, in the Arteris NoC, “the pressure information used to define the preferred traffic class (QoS) of the requesting inputs... [t]he pressure information is given top priority by the switch arbiter” and “the input controller extracts pertinent data from packet headers, forwards it to the routing table, fetches back the target output number, and then sends a request to the arbiter. After arbitration is granted, the input controller transmits the rest of the packet to the crossbar. The request to the arbiter is sustained as long as the last word of the packet has not been transferred. Upon transferring the last cell of the packet, the arbiter is allowed to select a new input.”</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 321, 322.</p>
<p>the resource manager responding with the availability of the target connection to the communication manager; and</p>	<p>In the Arteris NoC in the Snapdragon SoC included in the Samsung product, the resource manager responds with the availability of the target connection to the communication manager, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Snapdragon SoC included in the Samsung product, “the pressure information used to define the preferred traffic class (QoS) of the requesting inputs... [t]he pressure information is given top priority by the switch arbiter” and “the input controller extracts pertinent data from packet headers, forwards it to the routing table, fetches back the target output number, and then sends a request to the arbiter. After arbitration is granted, the input controller transmits the rest of the packet to the crossbar. The request to the arbiter is sustained as long as the last word of the packet has not been transferred. Upon transferring the last cell of the packet, the arbiter is allowed to select a new input.”</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 321, 322.</p>

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	<p>As a further illustration, in the Arteris NoC, “[t]he arbiter ensures that the connection matrix (a row per input and a column per output) contains at most one connection per column, that is, a given output is not fed by two inputs at the same time. The dual guarantee – at most one connection per row – is handled by the input controller. Each output has an arbiter that includes prefiltering. For maximum flexibility, each port can specify its own arbiter from the list of available arbiters (random, round robin, LRU, FIFO, or fixed priority).”</p> <p><i>Id.</i> at 322-323.</p>
the target connection between the first and second module being established based on the available properties of said communication channels of said connection.	<p>In the Arteris NoC in the Snapdragon SoC included in the Samsung product, the target connection between the first and second module is established based on the available properties of said communication channels of said connection, either literally or under the doctrine of equivalents.</p> <p>For example, in the Arteris NoC used by the Snapdragon SoC included in the Samsung product, “QoS is supported in the switch” which “choos[es] the route” using a “routing table”; “arbitrat[es]”; and “switch[es]”:</p>

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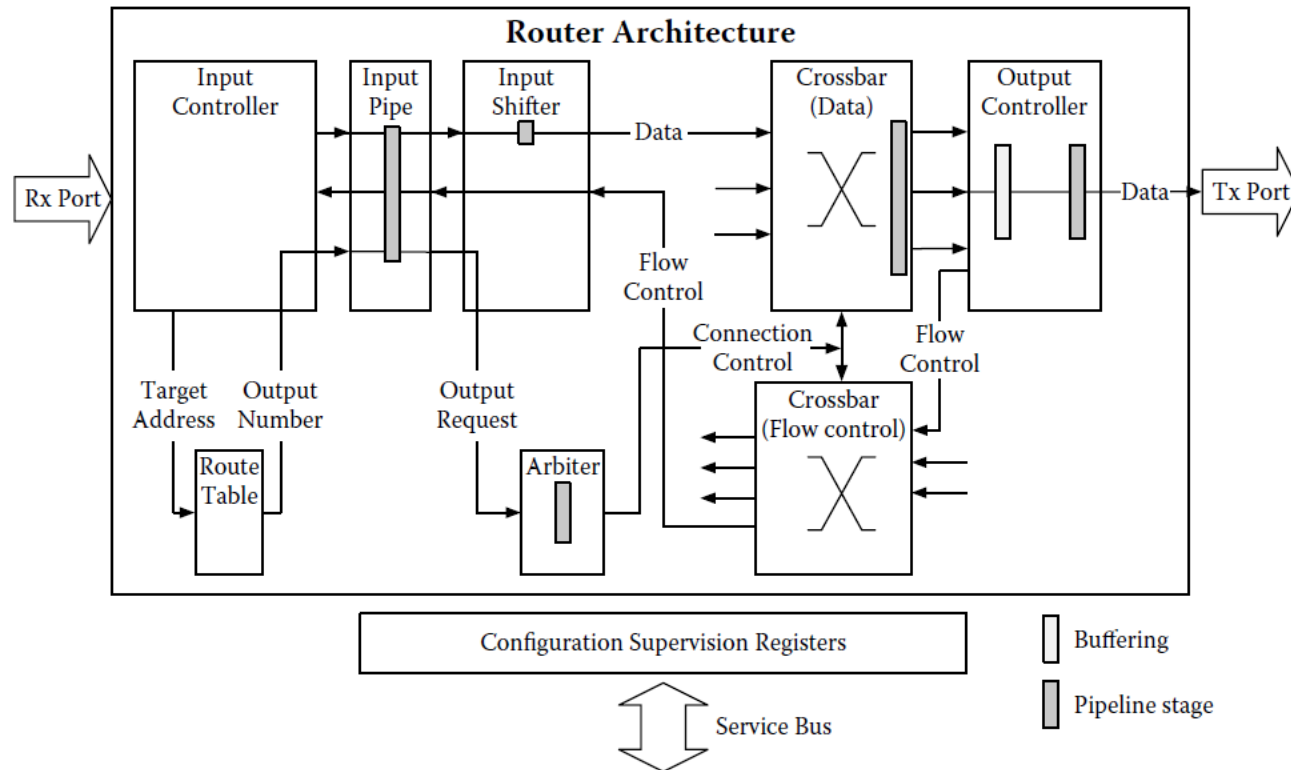
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Packet transportation unit: Router architecture.

See Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 319-320.

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